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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,784	03/04/2004	Takahiro Ohkuma	Y0647.0147	5197

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EXAMINER	
CEHIC, KENAN	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,784	OHKUMA, TAKAHIRO	
	Examiner	Art Unit	
	Kenan Cehic	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/04/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

DATA#0 and DATA#1 of Figure 3 are never mentioned in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al (US 6,728,271 B1) in view of Lim et al (US 2004/0160898 A1). Hereinafter referred as Kawamura and Lim.

For claim 1, Kawamura discloses a packet processing circuit comprising (see Figure 7) : a plurality of macros (see Figure 7, reference signs 10,13,16) each of which processes packet data (see Figure 7, reference signs 10,13,16 (packet header and payload are processed, see also column 1 line 65 – column 2 line 13) on the basis of a clock (see column 2 lines 12-22, unit processes packets based on a synchronous clock) and outputs the processed packet data (see column 2 lines 8-14, packet parts are processed) from at least one route, said macros being cascade-connected (see Figure 7, reference signs 10,13,16, note interconnections); and a clock supply unit (see Figure 7, reference 25) which supplies the clock to a macro to be controlled (see Figure 7, note arrows from reference 25 to 10,13,16, titled "Synchronous Clock Signal") and, stops supplying the clock to said macro to be controlled (see column 2 lines 16-22).

For claim 2, wherein said clock supply unit (see Figure 7, reference 25) comprises a clock which supplies the clock to said macro to be controlled buffer (see Figure 17, see especially references 30-36, this is logic circuit which stores (which is what a buffer

does) and processes a clock signal and provides it to the packet processing units 10,13,51,52,16), and a clock management unit (see Figure 7, reference 25 and Figure 17) which causes said clock buffer corresponding to said macro to be controlled to stop supplying the clock (see column 2 lines 16-22).

For claim 3, Kawamura teaches wherein said macro on the input side comprises a first signal output unit (see Figure 7, reference 10, this unit functions as a timing signal output unit) which outputs, to said clock management unit (see Figure 7 note arrows ("Packet start signal") from processing units 10, 13, 16 to "Clock supply controlling unit"), a first packet output notification signal (see Figure 7 note arrows ("Packet start signal") and column 8 lines 44-46) which indicates that the packet data is output (see column 8 lines 44-46), and

said clock management unit comprises a packet output detection unit (see Figure 17, especially reference 32) which causes said clock buffer to start supplying the clock when the first packet output notification signal is enabled and stop supplying the clock when the first packet output notification signal is not enabled (see column 11 lines 26-33, when a packet start signal is received, clock is provided, and conversely when the signal is provided, clock is not provided).

For claim 4, Kawamura teaches wherein said packet output detection unit comprises a counter circuit (see Figure 17, references 32a-b) which detects the predetermined time by counting the number of clocks (see column 17 line 64 - column 18 line 1), said counter

circuit resetting a count value (see column 17 lines 64-66, the counter counts each time to specific value).

For claim 5, Kawamura teaches wherein said counter circuit (see Figure 17, references 32a-b) detects the predetermined time by counting the number of clocks necessary (see column 17 lines 64-66, counter counts specific number of clocks) until the packet data passes through said macro on the input side (see column 17 line 64 - column 18 line 1, counter counts the number clocks needed to process through each unit).

For claim 6, Kawamura teaches aid macro on the input side comprises a plurality of routes (see Figure 15, arrows between "Header processing unit" and "Signal selection unit" indicated multiple paths) to output the processed packet data (see column 2 lines 8-14, packet parts are processed), and said first signal output unit (see Figure 7, reference 10, this unit functions as a timing signal output unit) outputs, to said clock management unit unit (see Figure 7 note arrows ("Packet start signal") from processing units 10, 13, 16 to "Clock supply controlling unit"), a first packet output notification signal which indicates that the packet data is output from at least one of the routes signal (see see Figure 7 note arrows ("Packet start signal") and column 8 lines 44-46, packet is transmitted over a stream).

For claims 1-6, Kawamura does not teach that no packet is output for a predetermined time and received on the input side of the macro. Lim from the same or similar field of

endeavor, teaches when no packet data is output (see section 0031) for a predetermined time (see section 0031, modules stayed powered up after a couple of cycles which equals a certain time period) from all routes (see Figure 1, note multiple input paths; see Figure 3, arrow entitled "All RXs are in idle state", note the plural meaning that no activity is on any paths) of a macro (see Figure 1, See RX and TX modules) on an input side (see section 0008) of said macro to be controlled.

For claim 4, Kawamura does not teach that the counting is reset when a signal is received. Lim from the same or similar field of endeavor teaches when the first packet output notification signal is turned on (see section 0006).

Thus it would have been obvious to a person of ordinary skill at the time the invention was made to combine the feature of a predetermined time of inactivity turn off by Lim, to the method of stopping the clock supply as taught by Kawamura. Both inventions deal with packets processing devices and saving / turning off power or clock supply when it is not needed. Thus one could have implemented the method of Lim into the system Kawamura additional digital circuitry. For example one could have implemented that the counters in Figure 17 by Kawamura, to count for a predetermined time (which Kawamura discloses), when "Packet start signal" signal is not received. Specifically, for claim 4 one could have included, via additionally circuitry, the signal, that shows that there is no activity an all the RX lines, into the processing units as taught by Kawamura. Furthermore, that signal could have been feed into the counters of Figure 17 as taught by Kawamura, in order to reset them.

The motivation for claim 1-6 is that with the combination of these methods the power requirement is reduced, when the processing units / device is not being actively used (as suggested by Lim, see section 0003 and Kawamura see section 2 lines 32-34)

Allowable Subject Matter

6. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Additionally, the objection set forth in this office action needs to be overcome.

While prior art teaches two signal units and where these two signals are ORed (Figure 17 of Kawamura et al (US 6,728,271 B1)), it does not teach that this second signal is related to output of the packet data.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US-4,316,247 A	Iwamoto, Eisaburo
US-4,698,748 A	Juzswik et al.
US-2002/0007463 A1	Fung, Henry T.
US-2006/0059377 A1	Sherburne, Robert Warren JR.
US-2006/0259797 A1	Fung, Henry T.

The above references are cited to show method of power conservation and clock reduction or shut off.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenan Cehic whose telephone number is (571) 270-3120. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton can be reached on (571) 272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KC

Ton

DANG T. TON
SUPERVISORY PATENT EXAMINER